

REMARKS

Applicant thanks the Examiner for indicating that claims 5-13, 16 and 17 contain allowable subject matter.

Applicant notes that an interview was conducted with the Examiner and his supervisor on September 10, 2003 in which it was believed by Applicants that the cited prior art, including the Yoshida reference, was overcome by the amendments later submitted on September 11, 2003. However, it appears that the Examiner has decided to maintain the rejection under Yoshida.

I. INTRODUCTION

Claims 1-3 and 5-17 are pending in the above application.

Claims 1-3, 14 and 14 stand rejected under 35 U.S.C. §102.

Claims 5-13, 16 and 17 stand allowed.

Claims 5-13, 16 and 17 are indicated as containing allowable subject matter.

Claims 1, 5, 6, 8, 12 and 16 are the independent claims.

II. PRIOR ART REJECTIONS

Claims 1, 2, 3, 14 and 15 stand rejected under 35 U.S.C. §102 as being anticipated by Yoshida (U.S. Patent 5,998,843), as set forth on pages 2-3 of the Office action.

Although this rejection was discussed in the interview, and it was Applicant's understanding that the rejection would not be maintained against these claims as they were amended, the Examiner has maintained the rejection. Applicant's respectfully traverse as follows:

Anticipation under 35 U.S.C. § 102 requires that *each and every element* of the claim be disclosed in a prior art reference as arranged in the claim. See, *C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1349, 48 U.S.P.Q.2D (BNA) 1225 (Fed. Cir. 1998), *Shearing v. Iolab Corp.*, 975

F.2d 1541, 1544-45, 24 U.S.P.Q.2D (BNA) 1133, 1136 (Fed. Cir. 1992); *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2D (BNA) 1913, 1920 (Fed. Cir. 1989); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 U.S.P.Q. (BNA) 481 (Fed. Cir. 1984); *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894, 221 U.S.P.Q. (BNA) 669, 673 (Fed. Cir. 1984); and *Connell v. Sears, Roebuck & Co.*, 220 USPQ 193, 198 (Fed. Cir. 1983).

Yoshida does not disclose each and every limitation of independent claim 1. Claim 1 recites a semiconductor device having a combination of elements including a “shallow trench isolation formed between the source/drain diffused layer and the dummy diffused layer, ... wherein the dummy diffused layer has its surface covered with an anti-silicidation film at least partially, on which no gate electrode is provided.” Yoshida does not disclose a semiconductor device which has a shallow trench isolation formed between the source/drain diffused layer and the dummy diffused layer which has its surface at least partially covered with an anti-silicidation film, as recited in claim 1.

The Office action appears to assert that “field oxidized films 5”, recited as being formed “using the LOCOS method” constitutes a “shallow trench isolation” (Office action pp. 3-4), as well as the “anti-silicidation film” (Office action pg. 2), both of which are recited in claim 1. Quite clearly, a single element in the Yoshida reference cannot be used to satisfy two distinct limitations in claim 1. Such proposition is the very antithesis of the requirement of meeting each and every limitation of the claims, *i.e.* all limitations in a claim must be considered meaningful. See, *Lantech Inc. v. Keip Manuf. Co.*, 32 F.3d 542, 546 (Fed. Cir. 1994); and *Lemelson v. United States*, 752 F.2d 1538, 1551 (Fed. Cir. 1985). Accordingly, Yoshida clearly does not

disclose each and every element of the above claims, and hence, does not anticipate the above claims.

Moreover, it is well established that the words used in the claims are examined through the viewing glass of a person skilled in the art. See, *Tegal Corp. v. Tokyo Electron Am., Inc.*, 257 F.3d 1331, 1342, 59 USPQ2d 1385, 1393 (Fed. Cir. 2001). See also, MPEP 2111, pg. 2100-47, “the broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach”, citing *In re Cortright*, 165 F.3d 1353, 1359 (Fed. Cir. 1999). The interpretation in the Office action that the “field oxidized films 5”, recited as being formed “using the LOCOS method” of Yoshida, would be understood by an artisan as a “trench isolation” is clearly contradicted by the evidence of record. Indeed, the very reference upon which the Office relies for such proposition, Wolf, after describing various LOCOS techniques for over 20 pages, expressly states in a bolded heading”

2.6 NON-LOCOS ISOLATION TECHNOLOGIES, I: (TRENCH ETCH AND REFILL)

Replacement of LOCOS as the isolation technology for like devices within the same tub in CMOS.

Wolf, SILICON PROCESSING FOR THE VLSI ERA, Vol. 2, Process Integration, pg. 45. The reference could not state any more clearly that trench isolation, as understood by one of skill in the art, is not a LOCOS technology.¹ As the Office cannot provide an interpretation of a claim term which contradicts its use in the art, the rejection cannot stand. See, MPEP 2111.

Moreover, rejection in the Office action appears to be based on a fundamental misunderstanding of the Yoshida reference and LOCOS isolation. The Office action asserts:

¹ Applicants note that a second reference can only be used in a §102 rejection for limited purposes, one of which is to explain the meaning of a term in the anticipation reference. See, MPEP 2131.01, pg. 2100-70. It is presumed that this is how the Office uses the Wolf reference. Any suggestion to modify the teachings of the Yoshida reference can only be presented in the context of §103 rejection.

While Yoshida is silent with respect to how the LOCOS isolation is formed, one having ordinary skill in the art would be aware that LOCOS isolation involves forming a shallow trench in the substrate and then growing thermal oxide to fill the trench. Another method of forming the LOCOS oxide, would involve forming a mask on a flat substrate and performing a thermal treatment to grow the oxide, which would also result in a shallow trench being formed since the underlying silicon is consumed.

Office action, pp. 3-4. First, contrary to the assertion in the Office action, Yoshida is not silent on how the “field oxidized films 5”, apparently referred to as the “LOCOS isolation” by the Office action, are formed. Indeed, the Yoshida makes it abundantly clear that the field oxidized films 5 are formed just after the epitaxial layer 4 is formed and prior to forming the n and p well regions, gate oxidized film 10 and polysilicon layer 27. See, col. 4, ll. 60-66; col. 5, ll. 65 – col. 6, ll. 4. Yoshida also illustrates that the field oxidized films 5 have a bulbous shape (Figs. 1-11), a shape which is known by the artisans to result from masked surface oxidation, as described in Wolf at page 20. Clearly, Yoshida is instructing one of skill in the art to mask regions on the epitaxial layer 4 and oxidize the unmasked surface regions, a process which is described by the Wolf reference as “the most widely used approach for forming the thick field oxide.” Wolf, pg. 19.

There is no suggestion in Yoshida to form a trench prior to oxidation, referred to as a “fully recessed oxide LOCOS process” in Wolf. Indeed, a fully recessed oxide LOCOS is described in Wolf as being distinctly characterized by a “bowl” shape (Wolf, pg 28, Fig. 2-14), contrary to the bulbous shape of a masked surface oxidation operation illustrated by Wolf (pg. 20, Fig. 2-6) which is depicted in Yoshida (Figs. 1-11). Moreover, to the extent that the Office action is suggesting that trenched LOCOS oxidation is the most common form of LOCOS oxidation, such that the term LOCOS would instruct the artisan to perform a trenched oxidation, such suggestion is clearly contradicted by the Wolf reference, which expressly states that masked surface oxidation is the most widely used form of LOCOS. Wolf, pg. 19. Moreover, after

reviewing the three paragraphs of problems affiliated with a trenched LOCOS operation, one of skill in the art would likely avoid using such technique (Wolf, pp. 30-31), *i.e.* far from being invoked in the artisan's mind with a mere mention of "LOCOS", its use would likely be a rare occurrence indeed. In any event, it is abundantly clear that the field oxidized film 5 in Yoshida is formed by a simple masked surface oxidation.²

Moreover, to the extent that the Office action is suggesting that simple consumption of silicon during an oxidation process constitutes "trench isolation", such suggestion would render decades of terminology in the semiconductor art devoid of any meaning at all. The Applicant respectfully notes that it is the artisans who choose their terminology for their own purposes – the terminology is not chosen for legal purposes in pursuing a patent. The USPTO and courts do not attempt to dictate to the artisans the terminology that should be used, regardless of how imperfect the chosen language of the artisans may be. For this reason, the drafters of the MPEP have dedicated numerous sections directed toward to construing terms in the claims as understood by one of skill in the art and even requiring the applicant to use terms in a manner consistent with their ordinary meaning in the art. See, MPEP 2111, 2111.01 and 2173.05.

Accordingly, at least for the above reasons, Yoshida does not disclose each and every element of the above claims and does not anticipate the above claims.

² Notably, the burden is on the Office to establish that a reference discloses all of the claimed limitations by degree of scientific certainty – speculation and probabilities does not satisfy this burden. See, MPEP §§ 2142 and 2143.

III. CONCLUSION

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

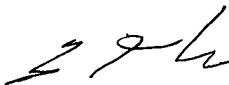
If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: February 20, 2004

By: 
Lawrence T. Cullen
Registration No.: 44,489

600 13th Street, N.W., Suite 1200
Washington, D.C. 20006-3096
Telephone: (202) 756-8000
Facsimile: (202) 756-8087
WDC99 877420-1.060188.0051